

REMARKS

Rejections under 35 U.S.C. §103

The Examiner has rejected Claims 1-20 under 35 U.S.C. §103(a) as being unpatentable over Nanja in view of Maitra in further view of Faucher, et al. (U.S. 5,404,543). Applicants respectfully disagree, but have Amended the claims to more particularly point out features of the present invention.

Claim 1 (and similarly Claims 7 and 15) recites:

"A method for managing energy use in a multi-threaded processing system, said method comprising:

first **measuring the per-thread usage of a device by each thread in a first set of multiple threads concurrently executing within said multi-threaded processing system**, said measured usage comprising an indicator for each of said multiple threads, **wherein said device is a device coupled to and external to a processor executing said first set of multiple threads;**

storing said measured per-thread usage for each of said first set of threads;

determining a next set of threads scheduled for execution;

retrieving previously-stored per-thread measured usage of said device corresponding to said next set of threads;

predicting a usage of said device by said next set of threads in conformity with said retrieved usage; and

sending a power management command to said device **in conformity with a result of said predicting**, whereby a power management state of said device is set in conformity with said previously-stored measured usage corresponding to said next set of threads." [bold text added for emphasis]

The present invention provides a mechanism that sets the power management state of a device coupled to a processor that concurrently executes multiple threads. The power management state of the device is set for a next set of threads to be concurrently executed by the processor. The power management state of the device is set in conformity with a predicted usage corresponding to the next set of threads. Thus the present invention provides a predictive mechanism for setting a next device power management state based on the historical use of the device by the threads forming the next set of threads.

Nanja and Maitra are both concerned with controlling the voltage and/or frequency of a processor core and not the power management states of external devices coupled to the processor. Further, Nanja, as noted by the Examiner in the Office Action, does not retrieve a per-thread device usage value for a next set of threads to be run. Neither does Maitra. Maitra in the passage cited by the Examiner at col. 8, line 45 through col. 9, line 10, discloses that the computing requirement of an application is retrieved from and is read from an initialization file. See Maitra col. 9, lines 45-53. While Maitra mentions that the initialization file can be obtained from benchmarks, that is not the same as, and does not suggest, the per-thread device usage that is measured, stored and retrieved as recited in the Claims.

Therefore Maitra does not predict device usage for a next set of threads from stored device usage values measured for those threads. Faucher, which does not disclose per-thread-set device control at all, further does not disclose or suggest the present invention in combination with Nanja and Maitra.

Therefore, for all of the reasons stated above, Applicants believe that the rejection under 35 U.S.C. §103(a) has been overcome.

Therefore, for all of the reasons stated above, applicants believe that all of the rejections and objections have been overcome.

CONCLUSION

In conclusion, Applicants respectfully submit that this Amendment is fully responsive to all aspects of the objections and rejections tendered by the Examiner in the Office Action. Applicants respectfully submit that they have persuasively demonstrated that the above-identified Patent Application, including Claims 1-20 are in condition for allowance, and such action is earnestly solicited.

No fees should be incurred by this Amendment, but if there are any fees incurred by this Amendment, please deduct them from IBM Deposit Account NO. 09-0447.

Respectfully Submitted,

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